REMARKS

Claims 1-22 are pending. Applicant amended independent claim 1 to add the feature, recited in claim 9, that the windows of registers are relatively and absolutely addressable per thread. Claim 9 was amended to remove that feature, and to clarify the claim. Applicant made similar amendments to independent claims 12 and 21, and claim 22.

Rejections under 35 U.S.C. § 101

The examiner rejected claims 1 and 21 under 35 U.S.C. §101 on the ground that the claimed invention is directed to non-statutory subject matter.

Specifically, with respect to claim 1, the examiner contends that the language of the claim: "raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment or machine which could result in a practical application producing a concrete, useful and tangible result." The examiner further contends that, for example, the language of "executing thread" includes freeware from the Internet, and that Internet is not tangible. The examiner also contended that no details regarding the language "maintaining execution threads in parallel multithreaded processor," which appears in the preamble of claim 1, were found in the body of the claim, and thus the examiner reads that language as maintaining the thread over the Internet.

Applicant traverses the examiner's rejection of independent claim 1 under 35 U.S.C. §101. Applicant disagrees with the examiner's characterization of the language of independent claim 1 and with the examiner's contentions regarding non-statutory subject of the claim.

Applicant's independent claim 1 recites "accessing, by an executing thread in the multithreaded processor, a register set organized into a plurality of windows of registers that are relatively and absolutely addressable per thread." Applicant's independent claim 1 is directed to an operation executed in a multithreaded processor including a register set. A multithreaded processor and a register set are both tangible elements. Thus, claim 1 recites a concrete, useful and tangible action, which is all that is necessary to make a claim statutory. The technological arts test argued by the examiner is not required to establish statutory subject matter but nevertheless is met at least by the features of a multithreaded processor and a register set. As for

the examiner's reference to freeware available on the Internet, the applicant notes that page 2, lines 13-15 of the specification merely describes that operating system software to control the overall operation of multiprocessors may be freely available (hence the term "freeware"). The applicant further notes that the Internet is a public communication network, and is very much tangible.

Accordingly, applicant's claim 1 is directed to a useful operation performed on tangible devices, producing a tangible result. Therefore, applicant's independent claim 1 is statutory.

As for applicant's independent claim 21, the examiner argued that the claim is not limited to tangible embodiments. Independent claim 21 recites, "[a] computer program product residing on a computer readable medium for managing execution of multiple threads in a multithreaded processor ... ."

The preamble of claim 21 is directed to a tangible embodiment, namely, a computer program product residing on a computer-readable medium. The applicant notes that the language in the preamble of claim 21 conforms to the conventional form widely used to recite computer program product claims. Such claims are regularly used and appear in numerous issued patents including, for example, recently issued U.S. Patent Nos. 6,961,787, 6,961,686, and 6,954,833.

With respect to the features recited in the body of claim 21, those features are similar to the features recited in independent claim 1, and are therefore directed to statutory subject matter for similar reasons as those provided with respect to independent claim 1.

Provisional Double Patenting Rejections

The examiner provisionally rejected claims 1, 12 and 21 under the judicially created doctrine of obviousness double patenting as being unpatentable over claims 18 and 2, respectively, of copending application No. 09/760,509.

Applicant will hold the examiner's provisional double patenting rejections of claims 1, 12 and 21 in abeyance upon an indication of allowable subject matter.

Rejections under 35 U.S.C. §102

The examiner rejected claim 1 under 35 U.S.C. §102(b) as being anticipated by Cheng et al. ("The Compiler for Supporting Mutlithreading in Cyclic Register Windows", 1996). The examiner also rejected claims 1-21 under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 5,870,597 to Panwar et al.

With respect to claim 9, the examiner argued that, "[a]s to claim 9, Panwar also included absolute address (see the physical addresses in col. 2, lines 53-65)." The applicant respectfully disagrees with the examiner's contention.

Applicant's amended claim 1, which includes a feature previously recited in claim 9, describes "accessing, by an executing thread in the multithreaded processor, a register set organized into a plurality of windows of registers that are relatively and absolutely addressable per thread." Thus, an executing thread can either access the register set using relative addressing or absolute addressing.

Panwar, on the other hand, describes a processor that speculatively executes instructions that specify logical addresses, and a processor that converts the logical addresses to physical addresses (Abstract). Particularly, as shown in Panwar's FIG. 3, a register set is divided into windows having 32 registers. Different processes or programs executing on a processor 102 can allocate their own independent window (col. 7, lines 43-47). Panwar further describes that programs executing on a processor 102 access registers through a typical naming convention, such as r0, r1, r2, ..., r30. The programs executing on Panwar's apparatus therefore use only relative (logical) addresses when specifying the desired registers that the programs are to access. The logical addresses specified by instructions comprising various executing processes are then processed by flattening logic 400, which maps the logical addresses used by the instructions to physical addresses to thereby enable the processor to access the desired registers (col. 8, lines 48-55).

At no point does Panwar disclose or suggest that the executing processes, or programs, specify the registers' actual physical address. Rather, the physical addresses are only subsequently determined when the logical addresses provided by the executing processes are

mapped to their corresponding physical address by the flattening logic 400. Accordingly, Panwar does not disclose "accessing, by an executing thread in the multithreaded processor, a register set organized into a plurality of windows of registers that are relatively and absolutely addressable per thread," as required by applicant's independent claim 1.

As for the Cheng reference which the examiner used to only reject old claim 1, Cheng describes a compilation technique that supports pipelining and multithreading. While Cheng briefly mentions using register windows, and organizing registers into different parts that may be accessed by either a calling procedure, a child procedure (i.e., callee), or other windows (see section 3, page 58), Cheng does not disclose how registers are accessed. At no point does Cheng explain whether registers are accessed using relative addressing or absolute addressing, and Cheng certainly does not disclose or suggest "accessing, by an executing thread in the multithreaded processor, a register set organized into a plurality of windows of registers that are relatively and absolutely addressable per thread," as required by applicant's independent claim 1.

Thus, since neither Panwar nor Cheng disclose or suggest, alone or in combination, at least the feature of "accessing, by an executing thread in the multithreaded processor, a register set organized into a plurality of windows of registers that are relatively and absolutely addressable per thread," applicant's independent claim 1 is therefore patentable over the cited art.

Claims 2-11 depend from independent claim 1 and are therefore patentable for at least the same reasons that independent claim 1 is patentable.

Independent claims 12 and 21 recite "a register set that is organized into a plurality of windows of registers that are relatively and absolutely addressable by an executable thread," or similar language. At least this feature is not disclosed by the cited art for reasons similar to those provided with respect to applicant's independent claim 1. Accordingly, independent claims 12 and 21 are patentable over the cited art.

Claims 13-20 depend from independent claim 12 and are therefore patentable for at least the same reasons as independent claim 12. Claim 22 depends from independent claim 21 and is therefore patentable for at least the same reasons as independent claim 21.

In addition, as noted, the examiner also rejected claim 7 as anticipated by Panwar. Specifically, the examiner argued that "[a]s to claim 7, Panwar also taught dual port memory (see the multiported memory in col. 1, lines 44-45)." (paragraph 18, page 8 of the Office Action).

Applicant's claim 7 describes "wherein the window registers are implemented using dual ported random access memories."

Panwar mentions in the section entitled "Cross-Reference to related Applications" that Panwar's patent document is related to application serial No. 08/882,175 entitled "System for Efficient implementation of Multi-Ported Logic FIFO Structures in a Processor" (col. 1, lines 43-46). However, at no point does Panwar disclose or suggest that its apparatus uses dual-port, or multi-port random access memory to implement the windows of registers, as required by applicant's claim 7. Accordingly, applicant's claim 7 is patentable over the cited art.

Applicant's claim 19 recites the feature of "wherein the window registers are provided using dual ported random access memories." At least this feature is not disclosed by the cited art for reasons similar to those provided with respect to applicant's claim 7. Accordingly, applicant's claim 19 is patentable over the cited art.

Furthermore, as also noted, the examiner rejected claim 10 as anticipated by Panwar. Specifically, the examiner argued that "[a]s to claim 10, Panwar also includes source field and destination field (see destination and source in col. 2, lines 66-67, col. 6, lines 1-5)." (paragraph 21, page 8 of the Office Action).

Applicant's claim 10 describes "wherein an absolute address of a register is directly specified in a source field or destination field of an instruction."

Panwar states at col. 2, line 66 – col. 3, line 3:

> The five-bit register addresses encoded in an instruction word specify the instruction's source registers and the destination register. These register specifiers are logical addresses that index registers within the current register window. (emphasis added)

Thus, Panwar explicitly provides that the source and destination registers are specified as logical (i.e., relative addresses). Panwar, therefore, does not disclose "wherein an absolute address of a register is directly specified in a source field or destination field of an instruction,"

as required by applicant's claim 10. As for the examiner's reference to col. 6, lines 1-5 of Panwar, that paragraph does not discuss at all source and destination fields in an instruction.

Accordingly, applicant's claim 10 is patentable over the cited art.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

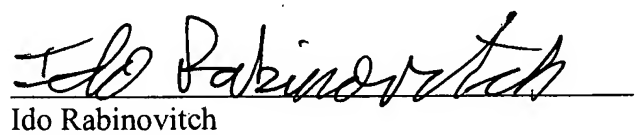
Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

In view of the foregoing remarks, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner's earliest convenience.

No fee is believed due. Please apply any charges to deposit account 06-1050, referencing attorney docket 10559-310US1.

Respectfully submitted,

Date: Nov. 23, 2005



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